

Description

METHOD OF FABRICATING A DUAL DAMASCENE COPPER WIRE

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a method of forming a dual damascene copper (Cu) wire, and more particularly, to a method of forming a dual damascene copper wire having superior Cu gap-filling ability and an enlarged process window.

[0003] 2. Description of the Prior Art

[0004] A dual damascene process is a method of forming a conductive wire coupled with a via plug in a dielectric layer. The dual damascene structure, comprising a trench and a via hole, is used to connect devices and wires in a semiconductor wafer within various layers and is isolated from other devices by the inter-layer dielectrics (ILD) around it. Since the resistivity of copper is smaller than the resistiv-

ity of aluminum (Al), a large current can be sustained in a small area. Consequently, chips having high speed, high integration, and high efficiency (with 30–40% improvement) are fabricated. To fill copper into the dual damascene structures thus becomes a trend in fabricating dual damascene copper wires. As integrated circuit technology advances, improving the yield of the dual damascene structure, simplifying the process flow and reducing the production cost are important issues in the manufacturing process of integrated circuits at the present time.

[0005] Please refer to Fig.1 to Fig.7. Fig.1 to Fig.7 are schematic diagrams of a method of fabricating a dual damascene copper wire according to the prior art. As shown in Fig.1, a semiconductor wafer 10 comprises a substrate 12, a conducting layer 14 disposed on a predetermined region of a surface of the substrate 12, and a passivation layer 16 composed of silicon nitride disposed on a surface of the conducting layer 14. Since the other elements disposed on the surface of the substrate 12 are not the concerning parts in the dual damascene process, they are not shown in Fig.1 and in other figures. Furthermore, the semiconductor wafer 10 comprises a low-k layer 18, a passivation layer 20, a low-k layer 22, and a hard mask

layer 24 sequentially disposed on a surface of the passivation layer 16.

[0006] The low-k layers 18 and 22 are normally formed of spin-on-coating (SOC) low-k materials, such as HSQ or FLARETM. Since many of the low-k materials (especially the organic low-k materials) are fragile, denser materials, such as silicon nitride, are chosen to form the passivation layer 20 on the low-k layer 18 to harden the low-k layer 18. Similarly, another passivation layer is required to cover the low-k layer 22. The hard mask layer 24 covering the low-k layer 22 functions not only as the passivation layer but also as a hard mask in subsequent etching processes. The hard mask layer 24 is composed of silicon nitride or silicon oxy-nitride.

[0007] As shown in Fig.2, after the stacked structure shown in Fig.1 is formed, a photolithographic and etching process is performed to form an opening 25 in the hard mask layer 24 until reaching a top surface of the low-k layer 22. The opening 25 defines a pattern for forming a trench of the dual damascene structure. Following this, as shown in Fig.3, a photo resist layer 26 is coated on the surface of the semiconductor wafer 10. Another photolithographic process is performed to form an opening 27 penetrating

through the photo resist layer 26 down to the top surface of the low-k layer 22. The opening 27 functions to define a pattern for forming a via hole of the dual damascene structure, so a width of the opening 27 must be smaller than that of the opening 25. In addition, the opening 27 is disposed inside the opening 25, such that a self-aligned contact (SAC) etching process is used thereafter to form the dual damascene structure.

[0008] As shown in Fig.4, a first etching process, such as an anisotropic dry etching process, is performed along the opening 27 to remove portions of the low-k layer 22 and the passivation layer 20 not covered by the photo resist layer 26, forming an opening 28 until reaching a top surface of the low-k layer 18. Thereafter, a resist stripping process is performed to completely remove the photo resist layer 26.

[0009] As shown in Fig.5, a second etching process is performed by utilizing the passivation layers 20 and 16 as stop layers to simultaneously remove portions of the low-k layers 22 and 18 not covered by the hard mask layer 24. Following this, both the passivation layer 20 and the passivation layer 16 not covered by the hard mask layer 24 are removed. As a result, a trench 30 penetrating through the

low-k layer 22 and the passivation layer 20, and a via hole 31 penetrating through the low-k layer 18 and the passivation layer 16 down to a top surface of the conducting layer 14 are simultaneously formed.

[0010] As shown in Fig.6, a deposition process is then performed to form a barrier layer 32 on the semiconductor wafer 10. The barrier layer 32 is formed of silicon nitride to prevent diffusion of copper or tungsten from various conductive layers into silicon. Alternatively, the barrier layer 32 can also be composed of composite materials such as silicon nitride/Ta/Ti/TiN to increase adhesion between the dual damascene structure and a metal layer covering the dual damascene structure. Following that, a re-sputtering process is performed to remove portions of the barrier layer 32 to expose the top surface of the conducting layer 14. A physical vapor deposition (PVD) process is thereafter performed to form a Cu seed layer 34 on the surface of the semiconductor wafer 10. The Cu seed layer 34 covers the exposed conducting layer 14 and the barrier layer 32. The objective for forming the Cu seed layer 34 is not only to provide a conductive path, but is also to provide a nucleation layer to allow the electric plating copper to nucleate and grow on it later. After that, an electric copper plating

(ECP) process is performed to form a metal layer 36 on a surface of the Cu seed layer 34 to fill up both the trench 30 and the via hole 31.

[0011] As shown in Fig.7, a chemical mechanical polishing process is performed by utilizing the barrier layer 32 as an end-point to remove the metal layer 36 and the Cu seed layer 34 disposed outside the trench 30 and the via hole 31, such that the remaining metal layer 36 inside the trench 30 and the via hole 31 is aligned with the surface of the barrier layer 32 disposed outside the trench 30. Finally, a passivation layer 38, such as a silicon nitride layer, is formed on the surface of the semiconductor wafer 10 to complete the fabrication of the dual damascene copper wire.

[0012] With regarding to the physical characteristics of the low-k material and the low resistivity copper wire, these two materials go together perfectly to effectively improve the RC delay caused by signal transmission between wires when the device size is shrunk. However, such a perfect combination faces a bottleneck. Since the Cu seed layer 34 is formed by a physical vapor deposition process, and the thin film formed by the physical vapor deposition process is characterized in poor step coverage, an overhang

phenomenon thus occurs to result in a discontinuous and not uniform Cu seed layer 34. As a result, voids are produced in the metal layer 36 when the metal layer 36 is filled into the dual damascene structure subsequently, leading to the poor Cu gap-filling problem. Due to the poor adhesion force between the Cu seed layer 34 and the barrier layer 32, peeling phenomenon occurs in the metal layer 36 during the subsequent chemical mechanical polishing process to decrease the yield of the dual damascene copper wire greatly. Please refer to Fig.8. Fig.8 is a schematic diagram illustrating defects produced in a dual damascene copper wire according to the prior art. As shown in Fig.8, the overhang phenomenon of the Cu seed layer 42 tends to occur at an open of the via hole 44, and the discontinuous phenomenon of the Cu seed layer 42 tends to occur at a bottom of the via hole 44. Therefore, the Cu seed layer 42 at the lower layer and the bottom layer grows slowly such that the bottom up filling behavior is not able to dominate the filling mechanism during the electric copper plating process. As a result, voids 48 are produced in the metal layer 46 after the electric copper plating process.

[0013] Therefore, it is very important to develop a new method of

forming a dual damascene copper wire to fill in the copper conductive layer into the dual damascene structure, having a small line width and a high aspect ratio, successfully without increasing the complexity of processing. In addition, this method should form the dual damascene copper wire having a low resistivity, a low surface roughness, and a superior adhesion.

SUMMARY OF INVENTION

[0014] It is therefore a primary objective of the present invention to provide a method of forming a dual damascene copper wire to resolve the above-mentioned problems.

[0015] According to the claimed invention, at least one wire is formed on a substrate. The substrate comprises at least one conductive region. An insulating layer is disposed on the substrate, and the insulating layer includes at least one recess exposing the conductive region. The method includes forming a barrier layer on a surface of the insulating layer and the recess, forming a continuous and uniform conductive layer on a surface of the barrier layer, forming a seed layer on a surface of the conductive layer, and forming a metal layer on a surface of the seed layer, and the metal layer filling up the recess.

[0016] Since the present invention method of forming the dual

damascene copper wire is to form the conductive layer, having good conductivity and good step coverage ability, underneath the Cu seed layer first, the thickness of the Cu seed layer is thus reduced to improve the overhang phenomenon of the Cu seed layer. Therefore, the continuity and uniformity of the Cu seed layer, and the adhesion between the Cu seed layer and the barrier layer are improved. Furthermore, because the conductive layer has superior continuity, uniformity, and current conductive ability, the overall conductivity uniformity is effectively improved to distribute the current evenly during the subsequent electric copper plating process. As a result, the Cu gap-filling ability is improved. Since the current conductivity on the conductive layer is very uniform, the process window of the subsequent electric copper plating process is obviously enlarged. When the Cu seed layer is an alloy layer, the metal atoms rather than the copper atoms will be absorbed to the grain boundaries to inhibit the diffusion of the copper atoms along the grain boundaries, leading to a greatly improved reliability performance.

[0017] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art

after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

- [0018] Fig.1 to Fig.7 are schematic diagrams of a prior art method of fabricating a dual damascene structure.
- [0019] Fig.8 is a schematic diagram illustrating defects produced in a dual damascene copper wire according to the prior art.
- [0020] Fig.9 to Fig.15 are schematic diagrams of a present invention method of fabricating a dual damascene copper wire.

DETAILED DESCRIPTION

- [0021] Please refer to Fig.9 to Fig.15. Fig.9 to Fig.15 are schematic diagrams of a present invention method of fabricating a dual damascene copper wire. As shown in Fig.9, a semiconductor wafer 100 comprises a substrate 102, a conducting layer 104 disposed on a predetermined region of a surface of the substrate 102, and a passivation layer 106 disposed on a surface of the conducting layer 104. Since the other elements disposed on the surface of the substrate 102 are not the concerning parts in the dual damascene process, they are not shown in Fig.9 to Fig.15.

Furthermore, the semiconductor wafer 100 comprises a low-k layer 108, a passivation layer 112, a low-k layer 114, and a hard mask layer 116 sequentially disposed on a surface of the passivation layer 106. The passivation layer 106, usually composed of silicon nitride, is used as an etch stop layer to avoid the materials underneath the via hole from being damaged when etching down to a bottom of the via hole due to over etch.

[0022] The low-k layers 108 and 114 are normally formed of spin-on-coating low-k materials, such as HSQ or FLARETM. In addition, the low-k layers 108 and 114 may be formed by a chemical vapor deposition (CVD) process. Since many of the low-k materials (especially the organic low-k materials) are fragile, denser materials, such as silicon nitride, are chosen to form the passivation layer 112 on the low-k layer 108 to harden the low-k layer 108. Similarly, another passivation layer is required to cover the low-k layer 114. The hard mask layer 116 covering the low-k layer 114 functions not only as the passivation layer but also as a hard mask in subsequent etching processes. The hard mask layer 116 is composed of silicon nitride or silicon oxy-nitride.

[0023] As shown in Fig.10, after the stacked structure shown in

Fig.9 is formed, a photolithographic and etching process is performed to form an opening 115 in the hard mask layer 116 until reaching a top surface of the low-k layer 114. The opening 115 defines a pattern for forming a trench of the dual damascene structure. Following this, as shown in Fig.11, a photo resist layer 118 is coated on the surface of the semiconductor wafer 100. Another photolithographic process is performed to form an opening 117 penetrating through the photo resist layer 118 down to the top surface of the low-k layer 114. The opening 117 functions to define a pattern for forming a via hole of the dual damascene structure, so a width of the opening 117 must be smaller than that of the opening 115. In addition, the opening 117 is disposed inside the opening 115, such that a self-aligned contact etching process is used thereafter to form the dual damascene structure.

[0024] As shown in Fig.12, a first etching process, such as an anisotropic dry etching process, is performed along the opening 117 to remove portions of the low-k layer 114 and the passivation layer 112 not covered by the photo resist layer 118, forming an opening 122 until reaching a top surface of the low-k layer 108. Thereafter, a resist stripping process is performed to completely remove the

photo resist layer 118.

[0025] As shown in Fig.13, a second etching process is performed by utilizing the passivation layers 112 and 106 as stop layers to simultaneously remove portions of the low-k layers 114 and 108 not covered by the hard mask layer 116. Following this, both the passivation layer 112 and the passivation layer 106 not covered by the hard mask layer 116 are removed. As a result, a trench 124 penetrating through the low-k layer 114 and the passivation layer 112, and a via hole 126 penetrating through the low-k layer 108 and the passivation layer 106 down to a top surface of the conducting layer 104 are simultaneously formed. In fact, the passivation layer 112 is also used as an etching stop layer to control the accuracy and uniformity of the thickness of the trench 124. When this etching stop layer is not disposed in the dual damascene structure, the non-uniformity of the dry etching process, the microloading effect, and the aspect ratio dependence etching (ARDE) effect tends to result in uncontrollable trench 124 thickness and trench 124 thickness uniformity.

[0026] As shown in Fig.14, a deposition process is then performed to form a barrier layer 128 on the semiconductor wafer 100. The barrier layer 128 is used for preventing

diffusion of copper or tungsten from various conductive layers into silicon. The barrier layer 128 may be a silicon nitride layer, a titanium nitride layer (TiN layer), a tantalum nitride layer (TaN layer), or a tantalum nitride/tantalum (TaN/Ta) composite metal layer. The barrier layer 128 is also used to increase adhesion between the dual damascene structure and a metal layer covering the dual damascene structure. Following that, a re-sputtering process is performed to remove portions of the barrier layer 128 to expose the top surface of the conducting layer 104.

[0027] A chemical vapor deposition (CVD) process or an atomic layer deposition (ALD) process is thereafter performed to form a continuous and uniform conductive layer 132 on a surface of the barrier layer 128 to cover the exposed conducting layer 104. The conductive layer 132 is usually an aluminum layer (Al layer) or a tungsten layer (W layer), and a thickness of the conductive layer 132 ranges from 5 to 400 angstroms (Å). Actually, any thin film, formed below 400°C, having good conductivity and step coverage ability, and having good adhesion to the barrier layer 128 can be used as the conductive layer 132.

[0028] After that, a physical vapor deposition process is per-

formed to form a Cu seed layer 134 on the surface of the semiconductor wafer 100. A thickness of the seed layer 134 ranges from 5 to 2000 angstroms, and the Cu seed layer 134 covers the conductive layer 132. The Cu seed layer 134 is composed of copper or copper alloy. The objective for forming the Cu seed layer 134 is not only to provide a conductive path, but is also to provide a nucleation layer to allow the electric plating copper to nucleate and grow on it later. An electric copper plating process is then performed to form a metal layer 136 on a surface of the Cu seed layer 134 to fill up both the trench 124 and the via hole 126.

[0029] Since the conductive layer 132 is formed prior to the Cu seed layer 134, and the conductive layer 132 formed by the chemical vapor deposition process or the atomic layer deposition process has a better step coverage ability, the thickness of the Cu seed layer 134 is decreased correspondingly. Therefore, the overhang phenomenon of the Cu seed layer 134 formed by the physical vapor deposition process is improved to improve the continuity and uniformity of the Cu seed layer 134, and to improve the adhesion to the barrier layer 128. In addition, because the conductive layer 132 has a very superior uniformity in

current conductivity, the overall conductivity uniformity is obviously improved to distribute the current evenly. As a result, the Cu gap-filling ability is improved.

[0030] As shown in Fig.15, a chemical mechanical polishing process is performed by utilizing the barrier layer 128 as an end-point to remove the metal layer 136, the Cu seed layer 134, and the conductive layer 132 disposed outside the trench 124 and the via hole 126, such that the remaining metal layer 136 inside the trench 124 and the via hole 126 is aligned with the surface of the barrier layer 128 disposed outside the trench 124. Finally, a passivation layer 138, such as a silicon nitride layer, is formed on the surface of the semiconductor wafer 100 to complete the fabrication of the dual damascene copper wire.

[0031] It is worth noticing that the conducting layer 104 is not limited to the shape and site shown in Fig.9 to Fig.15. Since the conducting layer 104 may be a source of a transistor, a gate of a transistor, a drain of a transistor, a lower level wire, a landing pad, or a resistor, its shape and site may change correspondingly. Furthermore, the present invention method is not only applied to a trench first dual damascene process shown in Fig.9 to 15, but is also applied to a via first dual damascene process. The via

first dual damascene process etches the copper plug pattern first, and then etches the copper wire pattern. The other portions of the via first dual damascene process is quite the same as the preferred embodiment of the present invention. The present invention method may also be applied to a self-aligned dual damascene process. The self-aligned dual damascene process is to form a hard mask layer composed of silicon nitride in the inter layer dielectric layer (ILD layer), and to etch a pattern required by forming the via hole in the hard mask layer. The other portions of the self-aligned dual damascene process is quite the same as the trench first dual damascene process and the via first dual damascene process. Moreover, the present invention method may be applied to a silicon-on-insulator substrate (SOI substrate).

[0032] Since the present invention method of forming the dual damascene copper wire is to form the conductive layer, having good conductivity and good step coverage ability, underneath the Cu seed layer first, the thickness of the Cu seed layer is reduced and the overhang phenomenon of the Cu seed layer is improved. Therefore, the continuity and uniformity of the Cu seed layer, and the adhesion between the Cu seed layer and the barrier layer are im-

proved. In addition, because the conductive layer has superior continuity, uniformity, and current conductive ability, the overall conductivity uniformity is effectively improved to distribute the current evenly during the subsequent electric copper plating process. As a result, the Cu gap-filling ability is improved. When applying the present invention method to a practical production line, the Cu gap-filling ability to the dual damascene structure having a small line width and a high aspect ratio is improved to fabricate the dual damascene copper wire having low resistivity, low surface roughness, and superior adhesion ability.

[0033] In contrast to the prior art method, the present invention method of forming the dual damascene copper wire is to form the conductive layer, having good conductivity and good step coverage ability, underneath the Cu seed layer first. The thickness of the Cu seed layer is thus reduced to improve the overhang phenomenon of the Cu seed layer. Therefore, the continuity and uniformity of the Cu seed layer, and the adhesion between the Cu seed layer and the barrier layer are improved. Furthermore, because the conductive layer has superior continuity, uniformity, and current conductive ability, the overall conductivity uniformity

is effectively improved to distribute the current evenly during the subsequent electric copper plating process. As a result, the Cu gap-filling ability is improved. Since the current conductivity on the conductive layer is very uniform, the process window of the subsequent electric copper plating process is obviously enlarged. When the Cu seed layer is an alloy layer, the metal atoms rather than the copper atoms will be absorbed to the grain boundaries to inhibit the diffusion of the copper atoms along the grain boundaries, leading to a greatly improved reliability performance.

[0034] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.